IN THE CLAIMS

1. (Original) In an interface circuit of a data storage system, a method for exchanging data with a volatile memory cache circuit, the method comprising the steps of:

providing a command to the volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit;

moving a data element through the point-to-point channel in accordance with the command; and

receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

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2. (Original) The method of claim 1 wherein the point-to-point channel includes a set of unidirectional links that carries signals from the interface circuit to the volatile memory cache circuit, and wherein the step of providing the command to the volatile memory cache circuit includes the step of:

sending the command to the volatile memory cache circuit through the set of unidirectional links of the point-to-point channel.

3. (Original) The method of claim 2 wherein the point-to-point channel further includes another set of unidirectional links that carries signals from the volatile memory cache circuit to the interface circuit, and wherein the step of receiving status from the volatile memory cache circuit includes the step of:

obtaining the status from the volatile memory cache circuit through the other set of unidirectional links of the point-to-point channel.

4. (Original) The method of claim 1 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit; and wherein the step of moving the data element includes the steps of:

sending the data element to the volatile memory cache circuit through the first set of unidirectional serial links when the command indicates a write transaction; and

obtaining the data element from the volatile memory cache circuit through the second set of unidirectional serial links when the command indicates a read transaction.

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5. (Original) The method of claim 4 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link; wherein the step of sending includes the step of:

outputting a respective portion of the data element framed with synchronization delimiters to the volatile memory cache circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of obtaining includes the step of:

inputting a respective portion of the data element framed with synchronization delimiters from the volatile memory cache circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

6. (Original) The method of claim 4 wherein the step of sending includes the step of:

outputting a respective portion of the data element and a corresponding multiple bit error detection code to the volatile memory cache circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of obtaining includes the step of:

inputting a respective portion of the data element and a corresponding multiple bit error detection code from the volatile memory cache circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

7. (Original) The method of claim 4 wherein the step of sending includes the step of:

outputting portions of the data element as data codes through the first set of unidirectional serial links when the command indicates a write transaction;

wherein the step of obtaining includes the step of:

inputting portions of the data element as data codes through the second set of unidirectional serial links when the command indicates a read transaction; and

wherein the data codes belong to an 8B/10B encoding/decoding data space.

8. (Original) The method of claim 4, further comprising the step of:

receiving a busy signal from the volatile memory cache circuit through each of the second set of unidirectional serial links after the step of providing the command and before the step of moving the data element.

9. (Original) The method of claim 4 wherein the step of providing the command includes the step of:

sending a tag indicator to the volatile memory cache circuit through the first set of unidirectional serial links; and

wherein the step of receiving the status includes the step of:

obtaining a copy of the tag indicator from the volatile memory cache circuit through the second set of unidirectional serial links.

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10. (Original) The method of claim 1 wherein the step of moving the data element through the point-to-point channel includes the step of:

reading the data element from the volatile memory cache circuit; and

wherein the method further comprises the step of:

processing the read data element within the interface circuit during the step of receiving status from the volatile memory cache circuit.

11. (Original) In a volatile memory cache circuit of a data storage system, a method for exchanging data with an interface circuit, the method comprising the steps of:

receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit;

moving a data element through the point-to-point channel in accordance with the command; and

providing status to the interface circuit through the point-to-point channel in accordance with the data element.

12. (Original) The method of claim 11 wherein the point-to-point channel includes a set of unidirectional links that carries signals from the interface circuit to the volatile memory cache circuit, and wherein the step of receiving the command from the interface circuit includes the step of:

obtaining the command from the interface circuit through the set of unidirectional links of the point-to-point channel.

13. (Original) The method of claim 12 wherein the point-to-point channel further includes another set of unidirectional links that carries signals from the volatile memory cache circuit to the interface circuit, and wherein the step of providing status to the interface circuit includes the step of:

sending the status to the interface circuit through the other set of unidirectional links of the point-to-point channel.

14. (Original) The method of claim 11 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit; and wherein the step of moving the data element includes the steps of:

obtaining the data element from the interface circuit through the first set of unidirectional serial links when the command indicates a write transaction; and

sending the data element to the interface circuit through the second set of unidirectional serial links when the command indicates a read transaction.

15. (Original) The method of claim 14 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link; wherein the step of obtaining includes the step of:

inputting a respective portion of the data element framed with synchronization delimiters from the interface circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

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wherein the step of sending includes the step of:

outputting a respective portion of the data element framed with synchronization delimiters to the interface circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

16. (Original) The method of claim 14 wherein the step of obtaining includes the step of:

inputting a respective portion of the data element and a corresponding multiple bit error detection code from the interface circuit through each of the first set of unidirectional serial links when the command indicates a write transaction; and

wherein the step of sending includes the step of:

outputting a respective portion of the data element and a corresponding multiple bit error detection code to the interface circuit through each of the second set of unidirectional serial links when the command indicates a read transaction.

17. (Original) The method of claim 14 wherein the step of obtaining includes the step of:

inputting portions of the data element as data codes through the first set of unidirectional serial links when the command indicates a write transaction;

wherein the step of sending includes the step of:

outputting portions of the data element as data codes through the second set of unidirectional serial links when the command indicates a read transaction; and

wherein the data codes belong to an 8B/10B encoding/decoding data space.

18. (Original) The method of claim 14, further comprising the step of:

sending a busy signal to the interface circuit through each of the second set of unidirectional serial links after the step of receiving the command and before the step of moving the data element.

19. (Original) The method of claim 14 wherein the step of receiving the command includes the step of:

obtaining a tag indicator from the interface circuit through the first set of unidirectional serial links; and

wherein the step of providing status includes the step of:

sending a copy of the tag indicator to the interface circuit through the second set of unidirectional serial links.

20. (Currently Amended) The method of claim 11 wherein the step of moving the data element through the point-to-point channel includes the step of:

providing the data element to the interface circuit; and

wherein the step of providing the status to the interface circuit ~~message~~ includes the step of:

sending ~~the~~ a status message to the interface circuit, ~~such that~~ the status message including a tag originally obtained from the interface circuit during the step of receiving the command to enable the interface circuit to verify that the interface circuit is a proper recipient of the data element ~~includes (i) a non-reserved value as a tag indicator when the data element is valid, and (ii) a reserved value as the tag indicator when the data is invalid~~.

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21. (Original) A data storage system, comprising:

a volatile memory cache circuit that buffers data elements exchanged between a storage device and a host;

an interface circuit that operates as an interface between the volatile memory cache circuit and at least one of the storage device and the host; and

a point-to-point channel, interconnected between the volatile memory cache circuit to the interface circuit, that carries the data elements between the volatile memory cache circuit and the interface circuit.

22. (Original) The data storage system of claim 21 wherein the point-to-point channel includes a set of unidirectional links that is capable of carrying a command from the interface circuit to the volatile memory cache circuit.

23. (Original) The data storage system of claim 22 wherein the point-to-point channel further includes another set of unidirectional links that is capable of carrying status from the volatile memory cache circuit to the interface circuit.

24. (Original) The data storage system of claim 21 wherein the point-to-point channel includes a first set of unidirectional serial links that carries signals from the interface circuit to the volatile memory cache circuit, and a

second set of unidirectional serial links that carries signals from the volatile memory cache circuit to the interface circuit.

25. (Original) The data storage system of claim 24 wherein each of the first set of unidirectional serial links and each of the second set of unidirectional serial links is an asynchronous link; wherein the interface circuit is configured to provide a respective portion of a data element framed with synchronization delimiters to the volatile memory cache circuit through each of the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain a respective portion of a data element framed with synchronization delimiters from the volatile memory cache circuit through each of the second set of unidirectional serial links during a read transaction.

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26. (Original) The data storage system of claim 24 wherein the interface circuit is configured to provide a respective portion of a data element and a corresponding multiple bit error detection code to the volatile memory cache circuit through each of the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain a respective portion of a data element and a corresponding multiple bit error detection code from the volatile memory cache circuit through each of the second set of unidirectional serial links during a read transaction.

27. (Original) The data storage system of claim 26 wherein the interface circuit is configured to provide portions of a data element as data codes to the volatile memory cache circuit through the first set of unidirectional serial links during a write transaction; and wherein the interface circuit is configured to obtain portions of a data element as data codes from the volatile memory cache circuit through the second set of unidirectional

serial links during a read transaction; and wherein the data codes belong to an 8B/10B encoding/decoding data space.

28. (Original) The data storage system of claim 24 wherein the volatile memory cache circuit is configured to provide a busy signal to the interface circuit through each of the second set of unidirectional serial links after receiving a command and before a data element moves through the point-to-point channel.

29. (Original) The data storage system of claim 24 wherein the interface circuit is configured to provide a tag indicator to the volatile memory cache circuit through the first set of unidirectional serial links when providing a command to the volatile memory cache circuit; and wherein the volatile memory cache circuit is configured to provide a copy of the tag indicator to the interface circuit through the second set of unidirectional serial links when providing status to the interface circuit.

30. (Original) An interface circuit for a data storage system, comprising:

a first adaptor that couples to at least one of a storage device and a host;

a second adaptor that couples to a point-to-point channel leading to a volatile memory cache circuit which is capable of buffering data elements exchanged between the storage device and the host; and

a controller, coupled to the first adaptor and the second adaptor, that is configured to:

provide a command to the volatile memory cache circuit through the point-to-point channel;

move a data element between the interface circuit and the volatile memory cache circuit, through the point-to-point channel in accordance with the command; and

receive a status message from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

31. (Original) A volatile memory cache circuit for a data storage system, comprising:

an adaptor that couples to a point-to-point channel leading to an interface circuit which operates as an interface between the volatile memory cache circuit and at least one of a storage device and a host;

memory locations that are capable of buffering data elements exchanged between the storage device and the host; and

A1 a controller, coupled to the adaptor and the memory locations, that is configured to:

receive a command from the interface circuit through the point-to-point channel;

move a data element between the volatile memory cache circuit and the interface circuit, through the point-to-point channel in accordance with the command; and

provide a status message to the interface circuit through the point-to-point channel in accordance with the data element.

32. (Newly Added) The method of claim 1 wherein the point-to-point channel includes a first link and a second link, and wherein the step of moving the data element through the point-to-point channel includes the step of:

conveying a first half of the data element through the first link and a second half of the data element through the second link.

33. (Newly Added) The method of claim 32, further comprising the step of:

dividing the data element into the first half of the data element and the second half of the data element prior to the step of conveying,

wherein the step of conveying includes the steps of:

transmitting the first half of the data element from a first transmitter and concurrently transmitting the second half of the data element from a second transmitter.

34. (Newly Added) The method of claim 33, further comprising the step of:

prior to transmitting the first half of the data element and the second half of the data element, associating a tag within each of the first half of the data element and the second half of the data element so that the tag passes through each of the first link and the second link of the point-to-point channel.

35. (Newly Added) The method of claim 34 wherein the point-to-point channel further includes a third link and a fourth link, and wherein the step of receiving the status through the point-to-point channel includes the step of:

obtaining (i) a first half of a status message through the third link, and (ii) a second half of the status message through the fourth link, the first half of the status message having a copy of the tag associated with the first half of the data element and the second half of the status message having a copy of the tag associated with the second half of the data element to enable the interface circuit to verify transmission of the status message to a correct interface circuit among multiple interface circuits.

36. (Newly Added) The method of claim 11 wherein the point-to-point channel includes a first link and a second link, and wherein the step of moving the data element through the point-to-point channel includes the step of:

conveying a first half of the data element through the first link and a second half of the data element through the second link.

37. (Newly Added) The method of claim 36 wherein the step of conveying includes the steps of:

receiving the first half of the data element from a first transmitter of the interface circuit and concurrently receiving the second half of the data element from a second transmitter of the interface circuit, and

wherein the method further comprises the step of:

reconstructing the data element from the first half of the data element and the second half of the data element.

38. (Newly Added) The method of claim 37 wherein the point-to-point channel further includes a third link and a fourth link, and wherein the step of providing the status to the interface circuit includes the steps of:

extracting a tag from the first half of the data element and sending a first half of a status message to the interface circuit through the third link, the first half of the status message having a copy of the tag from the first half of the data element; and

extracting a tag from the second half of the data element and sending a second half of the status message to the interface circuit through the fourth link, the second half of the status message having a copy of the tag from the second half of the data element.

39. (Newly Added) The data storage system of claim 21 wherein the point-to-point channel includes a first link configured to carry first halves of the data elements and a second link configured to carry second halves of the data elements, wherein the interface circuit includes a first transmitter and a second transmitter configured to concurrently transmit the first and second halves of the data elements respectively through the first and second links.

40. (Newly Added) The data storage system of claim 39 wherein the interface circuit is configured to (i) associate tags with the data elements and transmit the tags to the volatile memory cache circuit with the data elements, and (ii) receive tags within status messages from the volatile memory cache circuit in response to the data elements to verify transmission of the status messages to a correct interface circuit among multiple interface circuits.

41. (Newly Added) The interface circuit of claim 30 wherein the point-to-point channel includes a first outgoing link, a second outgoing link, a first incoming link and a second incoming link; and wherein the second adaptor is a transceiver having:

a first transmitter configured to transmit first halves of data elements through the first outgoing link of the point-to-point channel;

a second transmitter configured to transmit second halves of data elements through the second outgoing link of the point-to-point channel;

a first receiver configured to receive first halves of other data elements through the first incoming link of the point-to-point channel; and

a second receiver configured to receive second halves of the other data elements through the second incoming link of the point-to-point channel.

42. (Newly Added) The volatile memory cache circuit of claim 31 wherein the point-to-point channel includes a first outgoing link, a second outgoing link, a first incoming link and a second incoming link; and wherein the adaptor is a transceiver having:

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a first transmitter configured to transmit first halves of data elements through the first outgoing link of the point-to-point channel;

a second transmitter configured to transmit second halves of data elements through the second outgoing link of the point-to-point channel;

a first receiver configured to receive first halves of other data elements through the first incoming link of the point-to-point channel; and

a second receiver configured to receive second halves of the other data elements through the second incoming link of the point-to-point channel.